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Applicant..... Rambus Inc.
Group Art Unit 2841
Examiner ..... Phan, T.
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Title: Multi-Channel Memory Architecture

#10/Appeal Brief 3.2

APPEAL BRIEF

To: Board of Patent Appeals and Interferences
Washington, D.C. 20231

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Pursuant to 37 C.F.R. §1.192, Applicant hereby submits an appeal brief for application 09/665,920. A Notice of Appeal was filed January 8, 2003. Accordingly, Applicant appeals to the Board of Patent Appeals and Interferences seeking review of the Examiner's rejections.

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(1) Real Party in Interest

The real party in interest is the Rambus Corporation, the assignee of all right and title to the subject invention.

(2) Related Appeals and Interferences

Appellant is not aware of any other appeals or interferences which will directly affect, be directly affected by, or otherwise have a bearing on the Board's decision to this pending appeal.

(3) Status of Claims

Claims 1-30 were originally submitted. Claims 9, 10, and 22 are canceled. Claims 31-38 were submitted in a previous response. Thus, claims 1-8, 11-21, and 23-38 stand rejected and are pending in this Application. All pending claims are set forth in the Appendix of Appealed Claims on page 20.

Claims 1-8, 11-21, and 23-38 stand rejected under 35 U.S.C. §103(a) as being anticipated by US Patent No. 5,943,573 to Wen (hereinafter "Wen"), in view of US Patent No. 4,567,545 to Mettler, Jr. (hereinafter "Mettler"), and U.S. Patent No. 6,049,467 to Tamarkin et al. (hereinafter "Tamarkin").

(4) Status of Amendments

All amendments have been entered, and are reflected in the Appendix of Appealed Claims.

(5) Summary of Invention

This invention concerns a memory architecture that includes a substrate having first and second opposite edges. Memory devices are disposed on the substrate. Multiple channels extend from the first edge to the second edge such that each of the multiple memory devices is coupled to one of the multiple channels. Fig. 2 of the subject application, reproduced below, illustrates a device such as this.

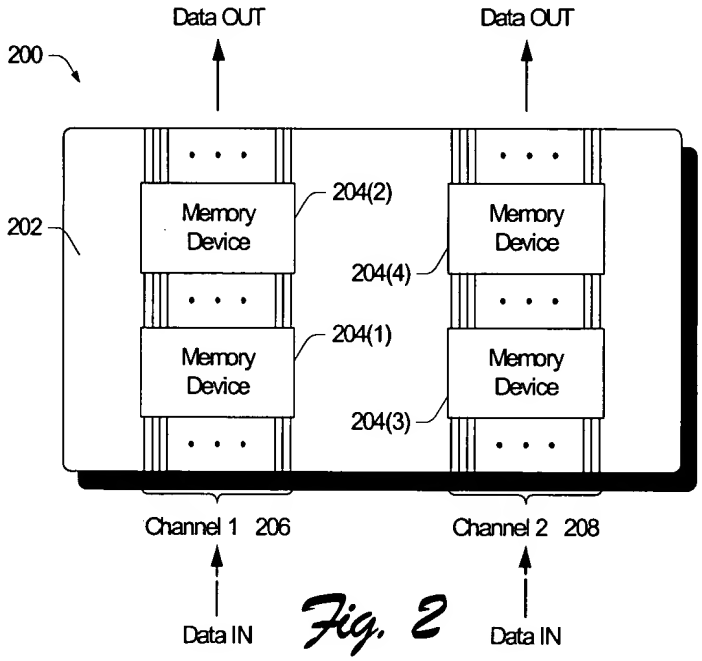

Fig. 2

In one embodiment, multiple channels extend across both sides of the substrate. Fig. 2 shows channel 1 206 and channel 2 208 extending across substrate 202. The lines that make up channel 1 206 and channel 2 205 represent conductors of the respective channels. As shown in Fig. 2, the channel conductors extend substantially linearly from one edge of substrate 202 to the opposite edge of the substrate. (*Specification*, Fig. 2 and Page 7, lines 3 to 5). Additional

channels may be located on the opposite side of substrate 202.

As shown, channel 1 206 is substantially the same length as channel 2 208. The two additional channels on the opposite side of substrate 202 are also substantially the same length as channels 206 and 208.

The opposite edges of substrate 202 have electrical contacts or pads that allow the channel conductors to communicate with other devices, such as a connector. (*Specification*, Page 7, lines 5 to 7). The connector is designed to receive an edge of the substrate and provide channel and channel conductor connectivity to other devices.

A number of memory devices can be coupled to each channel. In the illustrated example, channel 1 206 is coupled to memory devices 204(1) and 204(2), and channel 1 206 is coupled to memory devices 204(1) and 204(2). Four additional memory devices may be located opposite the four memory devices shown in Fig. 2. This configuration allows four memory devices 204 to be coupled to each of channels 206 and 208.

Fig. 7 of the subject application illustrates an embodiment where a connector couples multiple separate substrates.

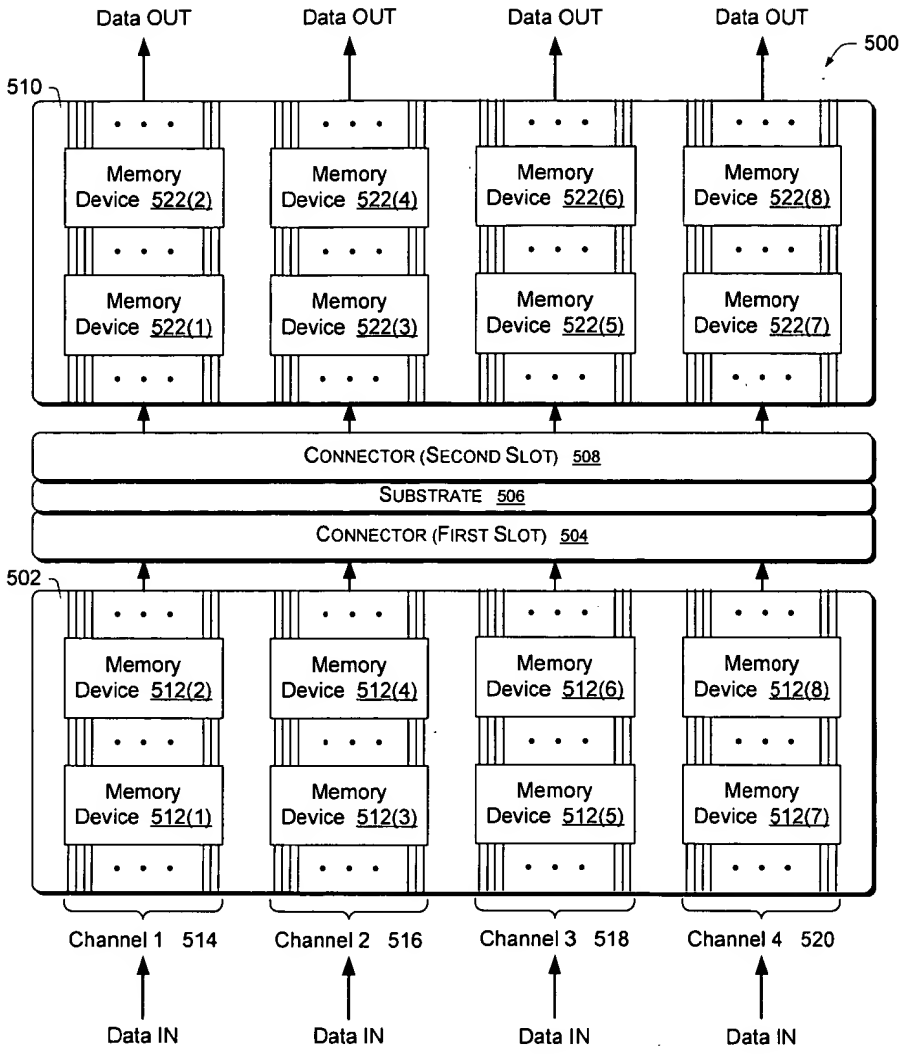

Fig. 7

Memory modules 502 and 510 have multiple channels 514, 516, 518, and 520 that extend across the memory modules. Memory module 502 is coupled to a first connector slot 504. The connector slot is coupled to a substrate 506, where substrate 506 may be a printed circuit board. Memory module 510 is connected to a second connector slot 508, which is similarly coupled to substrate 506. The substrate provides connectivity between the channels of the memory modules via connector slots 504 and 508, and thereby allows each channel to continue from one memory module to another.

Fig. 4 of the subject application illustrates an embodiment where connectors are used on both edges of a substrate.

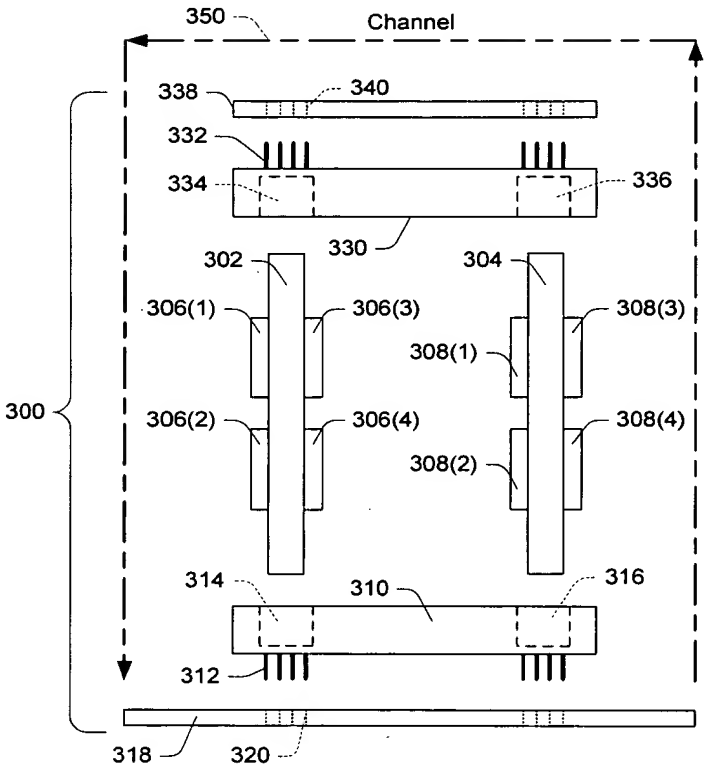

Fig. 4

Shown are two memory modules 302 and 304 similar to the memory module illustrated in Fig. 2. A first connector 310 is configured to receive an edge of memory modules 302 and 304, and a second connector connects the other edge of memory module 302 and 304. (*Specification*, Page 8, lines 11 to 2, Page 9, lines 6 to 7). A substrate 338 may be coupled to connector 330. Substrate 338 has multiple conductors that correspond to channel conductors of memory modules 302 and 304. (*Specification*, Page 9, lines 17-20). A single channel is established by the communication of connector 310, memory modules 302 and 304, connector 330 and substrate 338. The separate portions may be referred to as "channel

portions" that are combined to create "one" channel. (*Specification*, Page 10, lines 14 to 18). Path 350 is an example of a path that is formed from the channel portions. (*Specification*, Page 13, lines 19 to 20). The embodiment illustrated in Fig. 4 allows multiple substrates (i.e., memory modules 302 and 304) having multiple devices to be communicatively connected to one another.

The examples and embodiments described are illustrative. Although details of specific implementations and embodiments are described above, such details are intended to only to illustrate various features of the invention. The claims are not limited to the described embodiments.

(6) Issue

Whether claims 1-8, 11-21, and 23-38 are properly rejected under 35 U.S.C. §103(a) as being anticipated by Wen, in view of Mettler and Tamarkin?

(7) Grouping of Claims

Appellants respectfully submit that the rejected claims 1-8, 11-21, and 23-38 do not stand or fall together. The set of pending claims are separated into three groupings of claims. As is explained below, the groupings of the claims are separately patentable. However, it should be understood that the claim groupings below are presented for the purposes of isolating and reducing issues for this Appeal; thus, the claim groupings below should not be considered as the only groupings nor should individual claims be considered as consequentially not separately patentable.

A. Claims 1-6, 34-38.

B. Claims 7, 11-18.

C. Claims 19-21, 31-33.

D. Claims 8, 23-30.

(8) Argument

All of the submitted claims were rejected in the Office Action of 07/17/02 based upon three references: US Patent No. 5,943,573 to Wen (hereinafter "Wen"), US Patent No. 4,567,545 to Mettler, Jr. (hereinafter "Mettler"), and U.S. Patent No. 6,049,467 to Tamarkin et al. (hereinafter "Tamarkin").

Wen describes the fabrication of a semiconductor memory device having a typical memory layout in which word lines extend parallel to each other across a semiconductor die. Fig. 4D of Wen, to which the Office Action specifically refers, shows parallel word lines 43a and 43b. Note, however, that neither Fig. 4D nor any other of Wen's figures show any actual contacts for connection to external components. In fact, Wen specifically notes at col. 7, lines 21-25, that certain

steps, including formation of contacts, are not specifically described in the patent document. Thus, the Wen reference contains no teachings related to the location of contacts on a semiconductor die. The Office Action concedes that Wen does not disclose "electrical contacts at opposite edges of the substrate configured to allow communications through the channels via the electrical contacts, and connecting portions at both ends of the module." 07/17/02 Office Action, page 2, lines 21-24.

Mettler describes electrical contacts connected at an end of a substrate by a connector. Fig. 7 of Mettler, to which the Office Action refers, shows a single connector 52 at one edge of the substrate. Electrical leads (contacts) 22 that make up a set of leads (contacts) 48 extend from IC 26 to the single connector 52. A second set of leads (contacts) 54 from the IC 26 is wrapped around the substrate and is connected the single connector 52 (see col. 6, lines 9-12 of Mettler). The intent behind Mettler is to provide a single common connector located on a single edge that accesses the leads (channels) to the IC. Therefore, providing *electrical contacts at opposite edges* is not suggested by Mettler, and in fact goes against the teachings found in Mettler.

Tamarkin describes memory devices with contacts at opposite ends, but does not show a channel that passes through the memory devices. Fig. 2 of Tamarkin, to which the Office Action refers, shows a set of various random access memory (RAM) modules 24 connected to connectors 18, 20. Note, however, that neither Fig. 2 nor any other of Tamarkin's figures show any channels that connect the modules on the substrate and allow communications between the modules.

The following arguments are organized into four sub-arguments, one for each of the claim groupings.

(1) The Cited Combination of Wen, Mettler, and Tamarkin Does Not Teach or Suggest an Electrical Contacts at Opposite Edges To Allow Communications Between Devices Through Channels Via the Electrical Contacts.

All claims in grouping *A* (claims 1-6, 34-38) stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wen, Mettler, and Tamarkin.

Claim 1 is representative of claim grouping *A*. **Claim 1** recites in part:

> a plurality of memory devices disposed on the substrate;
>
> a plurality of channels extending between the opposite edges, wherein each of the plurality of memory devices is coupled to one of the plurality of channels; and
>
> electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts.

As discussed above, Wen does not disclose "electrical contacts at opposite edges of the substrate configured to allow communications through the channels via the electrical contacts, and connecting portions at both ends of the module."

As stated in the Office Action, Mettler teaches the use of a connector at "an" end of a substrate—at a single end of the substrate. Mettler, in fact, takes great pains to make sure that the connections are all at one end of the substrate, showing various techniques for wrapping conductors around substrate for use with a single connector. Thus, Mettler *teaches away* from the recited elements of claim 1, which include "electrical contacts at the opposite edges of the substrate." The law is clear that any reference that teaches away from a claimed feature in this

manner cannot be used in a combination purported to show the obviousness of the claimed feature. Thus, because Mettler explicitly teaches the need for all contacts to be at a single edge of a substrate, this reference highlights the *non-obviousness* of claim 1, which recites "electrical contacts at the opposite edges of the substrate." Mettler cannot fairly be said to establish the obviousness of electrical contacts at opposite edges of a substrate.

In addition to reciting contacts at opposite edges of a substrate, claim 1 recites a plurality of channels extending between the edges, wherein the electrical contacts at the opposite edges "allow communications through the channels via the electrical contacts." The Office Action does not establish any suggestions for such an element. As discussed above and conceded by the Office Action, Wen does not show electrical contacts, and Mettler shows an electrical connector only at one edge.

The Office Action recognizes these shortcomings of Wen and Mettler, citing Tamarkin for its disclosure of connectors at opposite ends of a substrate. However, there is nothing in Tamarkin to suggest the use of such connectors in conjunction with a structure having "channels extending between the opposite edges," wherein electrical contacts at opposite edges "allow communications through the channels via the electrical contacts," as recited by claim 1. There is no obvious combination of the three cited references which would satisfy these claim elements.

Specifically, there is nothing in any of the references that would have suggested utilizing connectors at each end of Wen's channels. The Examiner asserts that this would have been suggested by Tamarkin. However, Tamarkin's connectors are not used at either end of a channel. Furthermore, the cited art fails

to recognize any advantages or even any utility in using connectors at opposite ends of channels. In this regard, Wen does not even discuss connectors, while Tamarkin fails to utilize connectors that allow communications *through* such channels. The advantages of the claimed structure are apparent only in light of the Applicant's disclosure. Absent any recognition in the prior art of such advantages, it cannot be said that it would have been obvious to modify the references to result in the claimed structure.

The law is clear that any combination of references must be supported by a suggestion, in the references themselves, of the desirability of the combination:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.*"

MPEP, section 2142, 2100-108 (Rev. 3) (emphasis supplied).

In this case, the prior art discloses no advantages or utility for the proposed combination. Accordingly, the combination proposed by the Examiner would not have been obvious, and the rejection of claim 1 is unfounded. Allowance of claim 1 is respectfully requested.

Claims 2-6 of Group *A* all depend from claim 1, and are allowable because of their dependence from an allowable base claim. The remaining claims of Group *A* (claims 34-38) recite electrical contacts at opposite edges to allow communications between devices through channels via the electrical contacts and benefit from the same arguments of claim 1.

(2) **The Cited Combination of Wen, Mettler, and Tamarkin Does Not Teach or Suggest Multiple Substrates With Plurality of Devices that Are Communicatively Connected With One Another.**

All claims in grouping *B* (7, 11-18) stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wen, Mettler, and Tamarkin.

Claim 7 is representative of claim grouping *B*. Claim 7 is directed generally to first and second substrates and memory devices, as well as a connector that couples the channels of the two substrates.

Claim 7 recites in pertinent part:

> a first substrate having a plurality of memory devices disposed thereon and a first channel portion extending across the first substrate, the first substrate having opposite ends and contacts at the opposite ends to allow communications through the first channel portion via the contacts at the opposite ends of the first substrate;
>
> a second substrate having a plurality of memory devices disposed thereon and a second channel portion extending across the second substrate, the second substrate having opposite ends and contacts at the opposite ends to allow communications through the second channel portion via the contacts at the opposite ends of the second substrate; and
>
> a first connector configured to communicatively couple the first channel portion to the second channel portion through at least some of the contacts of the first and second substrates, wherein the first connector engages contacts at a first of the ends of the first substrate and engages contacts at a first of the ends of the second substrate.

The claimed first and second substrates are similar to the one discussed above with reference to claim 1, having channel portions and contacts at opposite ends, "to allow communications through the . . . channel portion[s] via the contacts at the opposite ends" of the substrates. Accordingly, claim 7 and its

dependent claims (8, 11-20) are allowable for the reasons discussed above with regard to claim grouping *A*.

In addition, claim 7 recites two such substrates and a particular connector configuration that couples the channel portions of the substrates. In rejecting this claim, the 07/17/2002 Office Action contends only that "to add additional substrate modules would have been an obvious design consideration based on the desired memory capacity." 07/17/2002 Office Action, Page 3, lines 21-22. However, the Office Action does not address how or why it would have been obvious to provide channel portions as recited and to couple with a connector as recited.

Wen describes a semiconductor memory device and does not discuss any sort of connectors. Mettler describes a connector at one end of a substrate, but does not describe coupling two substrates with a connector.

Tamarkin describes multiple connectors, but no arrangement whereby a channel portion on one substrate is coupled to a channel portion on another substrate.

Thus, even if it were somehow obvious to combine the teachings of these three references, there is no combination that would have used connectors to couple channel portions of two substrates as recited in claim 7. Importantly, the Office Action does not even propose any combination of references that would satisfy claim 7.

Accordingly, claim 7 cannot fairly be said to be obvious in light of the cited prior art, and should be allowed.

The remaining claims of Group *B* (claims 11-18) all depend from claim 7, and are allowable because of their dependence from an allowable base claim.

(3) The Cited Combination of Wen, Mettler, and Tamarkin Does Not Teach or Suggest Connectors on Both Ends of a Substrate.

All claims in grouping *C* (Claims 19-21, 31-33) stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wen, Mettler, and Tamarkin.

Claim 21 is representative of claim grouping *C*. Similar to the technology discussed above, claim 21 recites channel portions that extend across first and second memory modules having contacts at opposite ends. Claim 21 further is directed to connectors at both ends of the memory modules.

Claim 21 recites in pertinent part:

> a first connector coupling the first memory module to the second memory module through contacts at first ends of the first and second memory modules; and
>
> a second connector that engages contacts at the second ends of the first and second memory modules.

The Office Action does not address this element of claim 21, especially in the context set forth by the remaining portions of the claim. The Office Action does not identify any proposed combination of the references that would result in "a first connector coupling the first memory module to the second memory module through contacts at first ends of the first and second memory modules; and a second connector that engages contacts at the second ends of the first and second memory modules." (claim 21).

As discussed Tamarkin describes multiple connectors, but does not describe connectors at both ends of the memory modules (substrates) whereby channel portions extend across the memory modules with contacts at opposite ends.

Thus, the Office Action does not establish the obviousness of claim 21, and claim 21 should be allowed.

The remaining claims of Group *C* (claims 19-20, 31-33) recite connectors at both ends of the substrate and benefit from the same arguments of claim 21.

(4) The Cited Combination of Wen, Mettler, and Tamarkin Does Not Teach or Suggest Channel Portions That Are Coupled With One Another to Form a Channel.

All claims in grouping *D* (Claims 8, 23-30) stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wen, Mettler, and Tamarkin.

Claim 24 is representative of claim grouping *D*. Similar to the technology discussed above, claim 24 recites channel portions that extend between opposite edges of a substrate, and contacts at the opposite edges of the substrate to allow communication through the channel portions. Thus, claim 24 is allowable for many of the reasons already discussed. In addition, claim 24 recites:

> coupling together a pair of such substrates using a connector, a channel extending across the pair of substrates and the connector.

The Office Action does not address this element of claim 24, especially in the context set forth by the remaining portions of the claim. In particular, the Office Action does not identify any proposed combination of the references that would result in a "channel extending across the pair of substrates and the connector" (claim 24). Furthermore, none of the cited references show such a channel, created by coupling a pair of substrates with a connector.

Thus, the Office Action does not establish the obviousness of claim 24, and claim 24 should be allowed.

Claims 25-30 of Group *D* all depend from claim 24, and are allowable because of their dependence from an allowable base claim. The remaining claims of Group *D* (claims 8, 23) recite channel portions that are coupled to one another to form a channel and benefit from the same arguments of claim 24.

Conclusion

Applicant respectfully requests that the §103 rejection be withdrawn and that pending claims 1-8, 11-21, and 23-38 be allowed.

Respectfully Submitted,

Dated: 3/7/03

By: _____

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(9) Appendix of Appealed Claims

1. An apparatus comprising:

a substrate having first and second opposite edges;

a plurality of memory devices disposed on the substrate;

a plurality of channels extending between the opposite edges, wherein each of the plurality of memory devices is coupled to one of the plurality of channels; and

electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts.

2. An apparatus as recited in claim 1 wherein the substrate has a first side and a second side, the plurality of memory devices being disposed on both sides of the substrate.

3. An apparatus as recited in claim 1 wherein the substrate has a first side and a second side, the plurality of channels extending across both sides of the substrate.

4. An apparatus as recited in claim 1 wherein each channel includes a plurality of conductors, the plurality of conductors following a substantially linear path across the substrate.

5. An apparatus as recited in claim 1 wherein each channel includes a plurality of conductors, the plurality of conductors having lengths that are approximately equal.

6. An apparatus as recited in claim 1 wherein the substrate has one or more surfaces and the memory devices are mounted on such one or more surfaces of the substrate.

7. An apparatus comprising:

a first substrate having a plurality of memory devices disposed thereon and a first channel portion extending across the first substrate, the first substrate having opposite ends and contacts at the opposite ends to allow communications through the first channel portion via the contacts at the opposite ends of the first substrate;

a second substrate having a plurality of memory devices disposed thereon and a second channel portion extending across the second substrate, the second substrate having opposite ends and contacts at the opposite ends to allow communications through the second channel portion via the contacts at the opposite ends of the second substrate; and

a first connector configured to communicatively couple the first channel portion to the second channel portion through at least some of the contacts of the first and second substrates, wherein the first connector engages contacts at a first of the ends of the first substrate and engages contacts at a first of the ends of the second substrate.

8. An apparatus as recited in claim 7 wherein the coupling of the first channel portion to the second channel portion through the connector forms a channel.

11. An apparatus as recited in claim 7 wherein the first channel portion includes a plurality of conductors following a substantially linear path across the first substrate.

12. An apparatus as recited in claim 7 wherein the second channel portion includes a plurality of conductors following a substantially linear path across the second substrate.

13. An apparatus as recited in claim 7 wherein the first channel portion includes a plurality of conductors having lengths that are approximately equal.

14. An apparatus as recited in claim 7 wherein the second channel portion includes a plurality of conductors having lengths that are approximately equal.

15. An apparatus as recited in claim 7 further including a third substrate coupled to the first connector.

16. An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate.

17. An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate, the third

channel portion including a plurality of conductors following a substantially linear path across the third substrate.

18. An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate, the third channel portion including a plurality of conductors having lengths that are approximately equal.

19. An apparatus as recited in claim 7 further including a second connector that engages contacts at a second of the ends of the first substrate and engages contacts at a second of the ends of the second substrate.

20. An apparatus as recited in claim 19 wherein the second connector is coupled to a motherboard.

21. An apparatus comprising:

a motherboard; and

a first memory module having contacts at opposite ends thereof, a first channel portion extending across the first memory module between the contacts;

a second memory module having contacts at opposite ends thereof, a second channel portion extending across the second memory module between the contacts;

a first connector coupling the first memory module to the second memory module through contacts at first ends of the first and second memory modules; and

a second connector that engages contacts at the second ends of the first and second memory modules.

23. An apparatus as recited in claim 21 wherein a channel extends across the first memory module, the second memory module, and the first connector.

24. A method comprising:

arranging channel portions on a substrate such that the channel portions extend between opposite edges of the substrate;

arranging contacts at the opposite edges of the substrate to allow communication through the channel portions;

arranging channel portion conductors such that the length of the channel portion conductors between opposite edges of the substrate is approximately equal; and

coupling together a pair of such substrates using a connector, a channel extending across the pair of substrates and the connector.

25. A method as recited in claim 24 further including propagating signals through the channel.

26. A method as recited in claim 24 further including arranging a plurality of memory devices on the substrate such that each memory device is coupled to a channel portion.

27. A method as recited in claim 26 further including propagating signals through the channel portions to perform memory operations.

28. A method as recited in claim 24 wherein each channel portion includes a plurality of conductors, each of the conductors having approximately equal lengths along the entire length of the channel portion.

29. A method as recited in claim 24 wherein each channel portion includes a plurality of conductors following a substantially linear path across the substrate.

30. A method as recited in claim 24 wherein channel portions are arranged on both sides of the substrate.

31. A memory system comprising:

first and second memory modules;

each of the first and second memory modules having contacts at first and second opposite ends thereof and having one or more communication channel portions extending between the contacts;

each of the first and second memory modules having a surface and one or more memory devices mounted to the surface, the one or more memory devices being communicatively coupled to the one or more communication channel portions;

one or more board connectors that engage the contacts at the first ends of the first and second memory modules to allow communications through the one or more communication channel portions of the memory modules;

a coupling that engages the contacts at the second ends of the first and second memory modules, the coupling being configured to communicatively couple the one or more channel portions of the first and second memory modules and to thereby form one or more communication channels that each comprise at least one of the communication channel portions of the first memory module and at least one of the communication channel portions of the second memory module.

32. A memory system as recited in claim 31, wherein the communication channel portions comprises a plurality of conductors following substantially linear paths across the respective memory modules.

33. A memory system as recited in claim 31, wherein each communication channel portion comprises a plurality of conductors having lengths that are approximately equal.

34. A memory module comprising:

a substrate having opposite ends and at least one surface;

contacts at the opposite ends of the substrate;

one or more memory devices mounted to the surface of the substrate; and

one or more communication channel portions extending across the module between the contacts, the one or more communication channel portions being

configured to allow communications through the contacts with the one or more memory devices.

35. A memory module as recited in claim 34, wherein the substrate has opposing surfaces, and the one or more memory devices comprise at least one memory device mounted on each of the opposing surfaces of the substrate.

36. A memory module as recited in claim 34, wherein the substrate has opposing surfaces, and the one or more communication channel portions comprise at least one communication channel portion extending across each of the opposing surfaces of the substrate.

37. A memory module as recited in claim 34, wherein each communication channel portion comprises a plurality of conductors that follow a substantially linear path across the substrate.

38. A memory module as recited in claim 34, wherein each communication channel portion comprises a plurality of conductors having lengths that are approximately equal.